

High-Power Polyphase PCB-Type Inductive Coupler for Wireless Electric Vehicle Charging

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Abstract—The cost and manufacturing difficulty of traditionally wound coils for wireless charging of electric vehicles has led to the exploration of alternative manufacturing for scalable deployment at a range of rated powers. A rotating-field polyphase wireless coupler is developed with balanced fully pitched coils which are not possible with conventional Litz wire. The usage of printed circuit board (PCB) technology is proposed for the innovative construction at large dimensions due to reduced cost, increased ease of manufacturability, and potential geometric customization compared to wound coils. Design considerations specific to PCBs are detailed for wireless power transfer coils including advantages such as the potential for many turns and transposition with planar interconnections. A design procedure is developed which may be used to investigate the frequency to power to dimension correlation and limits associated with PCB coils. Designs are simulated in 3D electromagnetic finite element analysis (FEA) for the polyphase coil to evaluate the coupling between coils with varying geometric parameters at 100mm and 500mm outer diameters. A discussion is included on methods to increase PCB power ratings through a mixture of layer stacking, connections, and material selection.

Index Terms—Wireless power transfer, planar coil, printed circuit board, Electric vehicle (EV), wireless charging, scalability

I. INTRODUCTION

Widespread adoption of wireless electric vehicle charging may be limited by the volume, weight, and manufacturing cost of traditional coils [1]. Litz wire, a multi-stranded wire made from thousands of individually insulated strands, is widely used for wireless power transfer (WPT) to mitigate skin effect and proximity losses with high current capability [2]. Litz wire has limited supplier availability and requires manual assembly, increasing the cost of inductive couplers for wireless charging [3]. Printed circuit boards (PCB) technology has been applied recently for electromagnetic device development including transformers and electric machines as presented in Kesgin *et al.* [4]. Benefits of using PCBs include significantly reduced volume, manufacturing modularity, repeatable fabrication processes, and flexibility in coil geometry.

Printed circuit boards are comprised of layers of copper plated onto a structural support, such as FR4 dielectric laminate, which are etched with acid to create conductive traces. Connections between layers are made with vias which are copper plated through-holes across planar layers. The usage of automated subtractive manufacturing allows for trace width

as big as desired and very customizable geometry. Conductor layouts have a high degree of flexibility due to a lack of minimum bend radius within planes and the perpendicular layer-to-layer connections. For PCB technology, this allows for the implementation of radial parallel splits as a replacement of parallel wires in conventional coils and axial parallel paths connecting coils across multiple layers. Typical PCBs have a high surface to volume ratio compared to traditional windings greatly increasing volumetric specific power density [5]. Multiple PCB modules can be connected within a stack to increase power output or for multiple phase excitation, benefiting from the small axial height. Techniques for manufacturing PCBs at large scale have significantly reduced cost relative to Litz wire due to demand across multiple industries.

Printed circuit board wireless charging coils have been proposed recently to capitalize on the benefits of a reduced volumetric envelope and manufacturing cost. Example papers include Chen *et al.* which analyzed coil loss within a 2D cross-section of a single layer square PCB [6]. Analytical equation-based design of square PCB coils was performed in Li *et al.* for PCB coils considering multiple layers connected in series [7]. A PCB coil receiver was designed, prototyped, and tested in Ramezani *et al.* at 85kHz, 3.3kW operation through a design with a mixture of 2D and 3D FEA [5]. A square PCB was developed at 3.3kW, 85kHz operation by Liu *et al.* with a focus on rapid prototyping and experimentation and suggested the potential for power as high as 11kW [3]. A comparative summary of example wireless charging coils is collected in Table I for a mixture of PCB and Litz wire coils with calculated receiver power densities in italics. The further development of PCB coils would benefit from a systematic analysis of the limitations and approaches for high power implementation considering multiple layers, modular PCBs, and the connections between them.

This paper proposes a polyphase PCB wireless charging coil with balanced full pole coverage coils enabled by geometry configuration not possible with Litz wire. A specialized PCB coil design procedure is developed considering manufacturing and materials limitations. Discussion is included for methods to increase rated power in PCB coils for wireless charging including radial and axial parallel connections, interleaving, and transposition. Finite element analysis (FEA) is employed for the design of the polyphase PCB wireless charging coil with

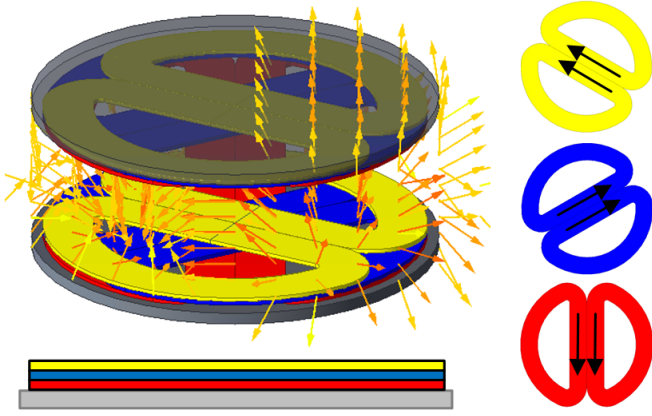


Fig. 1. Electromagnetic 3D FE model of the studied coil pair with example B-field vectors of the rotating electromagnetic field and the direction of current excitation per geometrically shifted phase coils.

TABLE I
EXAMPLE WIRELESS CHARGING COILS FROM LITERATURE

Parameters	[8]	[9]	[3]	[5]	[10]
Winding Material	Litz	Litz	PCB	PCB	PCB
Power [kW]	300	200	3.3	3.3	6.6
Frequency [kHz]	85	85	85	85	3125
Area [m^2]	1.51	0.44	0.12	0.30	0.13
Phases	3	1	1	1	1
Airgap [mm]	152	230	50	125	100
Surface Power Density [kW/m^2]	905	460	27	11	52
Volumetric Power Density [kW/dm^3]	27	-	7	1	17

multiple parametric sweeps to maximize coupling coefficient.

II. WIRELESS POWER TRANSFER COIL DESIGN METHODS

A polyphase rotating field coil, shown in Fig. 1, was selected for design due to the constant output power and high surface power density as previously reported in Pries *et al.* [11]. The direction of current excitation is as depicted in Fig. 1 with geometric rotation and electrical excitation shifted by 120° per phase. The B-field surface flux density plot in the ferrite in Fig. 2 is an example of the central flux concentration caused by the 3-phase rotating field.

The geometry features full pole coverage coils allowing for high copper area utilization and minimum flux leakage between poles. Practical implementation of this geometry is not possible with Litz wire due to unbalanced phase inductance and induced voltages because of varying distance to the ferrite core. The unique opportunities in PCB-based designs for planar transposition and customizable geometry has enabled further exploration of the three-layer three-phase polyphase coil within this paper.

An example polyphase WPT system is shown in Fig. 3 implemented with a three-phase inverter and diode rectifier including series compensation to minimize complexity. Voltage can be regulated passively with modified compensation circuit tuning, as done in [8], or actively on the secondary-side using buck-boost converters for high power CC-CV battery charging.

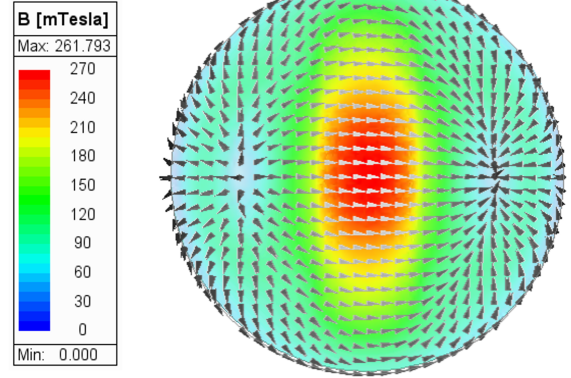


Fig. 2. Example simulation result of the primary-side ferrite surface flux density at a snapshot in time with the selected polyphase geometry. A central flux concentration is obtained by the rotating field produced by the 3 coils.

Initial sizing includes the definition of the airgap, rated power, induced voltage, and frequency, typically 85kHz for electric vehicle charging as defined in SAE J2954 [12]. The outer diameter (OD) can be selected based on the airgap length and the fundamental flux path which varies significantly per ferrite and coil geometry and largely determines the coupling coefficient, k , as summarized in Li and Mi [13]. Polarized coils, like the DD coils proposed by Budhia *et al.* [14], can achieve a minimum coupling coefficient across double the airgap as circular alternatives with the same outer diameter. The airgap to OD ratio for a satisfactory coupling coefficient should be determined per geometry with a parametric study varying the airgap similar to that performed in Fig. 7.

Typical design procedures, for example, those used in [15]–[17], define a mutual inductance limit at a coupling coefficient, between 0.15–0.20 for large airgaps, to determine the number of turns and the current is then selected for rated power. Remaining geometry parameters can then be determined with optimization of coupling coefficient and quality factor as performed in [10], [18] for power density and efficiency. Improvements to coupling coefficient reduce the self-inductance for a rated mutual inductance, which can decrease or increase the size of associated compensation components accordingly. The rated mutual inductance can be specified either by limiting the size of associated compensation components or considering a limited maximum current.

The conductor cross-section should initially be defined as the largest possible configuration smaller than the skin-depth to maximize current-carrying capability. Skin effect-induced eddy currents can be minimized by selecting conductor height and width smaller than the skin depth at the operating frequency with the equation:

$$\delta = 1/\sqrt{\pi f \mu \sigma} \quad (1)$$

where σ is the material conductivity, f is the operating frequency, and μ is the permeability of the material. A 1A current excitation should then be applied to the conductor

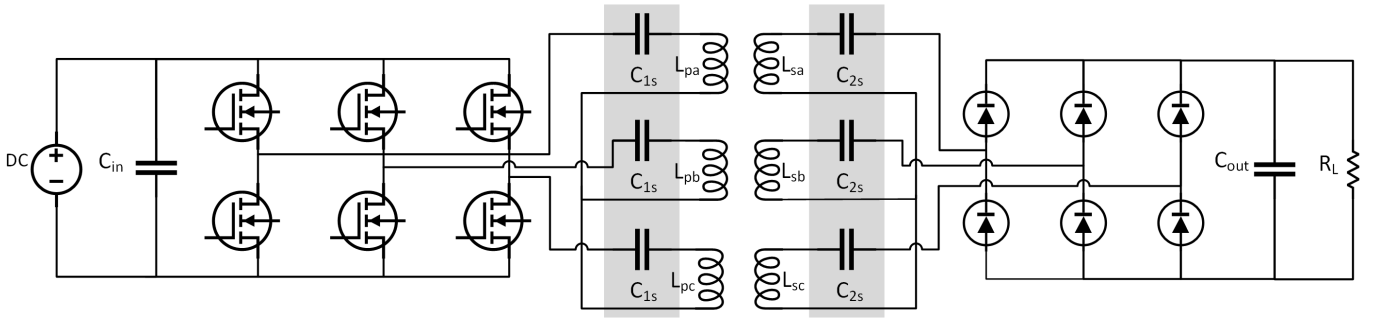


Fig. 3. Schematic for the proposed polyphase WPT system including a three-phase inverter, series-series compensation, and a diode rectifier. The simplest tuning method (series-series) is used to investigate the capability of designed coils to reach rated power.

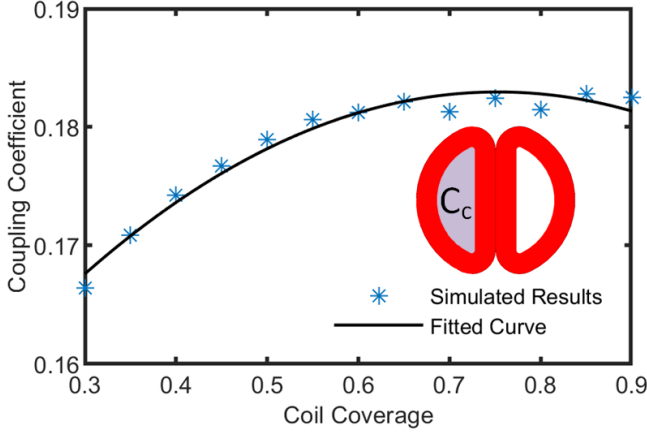


Fig. 4. Results of a parametric study of coil copper coverage, C_c , where coil width is the product of a quarter of the fixed outer diameter and coil coverage to evaluate the impact on coupling coefficient, k , at a fixed airgap.

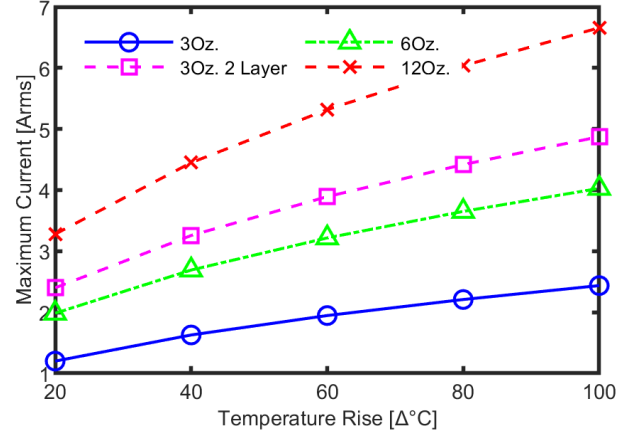


Fig. 5. Analytically derived maximum current excitation and maximum temperature change for a PCB coil without forced cooling and assuming a skin depth limited trace width of 0.22mm with different copper plate volumes.

with an initial estimate of the number of turns needed for the rated mutual inductance. Parametric studies have confirmed the independence of current with mutual and self-inductance, such that only a sweep of the number of turns is necessary to reach the necessary inductance for a pre-defined geometry.

Power within the selected geometry can be calculated with the following equation from Pries *et al.* [11]:

$$P = j\omega I_p^H \underline{M}_{ps} I_s = \frac{9}{2} \omega M_{ps} I_p I_s \quad (2)$$

where M_{ps} is the mutual inductance between the two coils, I_p is the current in the primary, and I_s is the current in the secondary. With the resulting mutual inductance, necessary current can be determined to achieve the rated power.

A parametric study of coil coverage, C_c , the portion of the interior coil that is covered, was also performed as generated magnetic flux limited to the portions where current is not actively excited. The results, shown in Fig. 4, found that the coupling coefficient only varies by 10% with a modification of the coil window, suggesting that coils with small windows are preferable for increased current capacity with planar parallel splits or increased number of turns. Additionally, the coupling coefficient within the explored coil was found to be negative between same side phase windings implying that the magnetic

field from phases add together instead of cancelling out as mentioned in [8]. Losses and the associated quality factor are determined in part by the current density, connection between coil paths, and coil geometry, requiring special consideration of the coupler materials.

III. SPECIFIC DESIGN CONSIDERATIONS FOR PCBs

Modifications to the coil design method were developed for the sizing of printed circuit board type coils considering technology specific size limitations and active manufacturing standards such as IPC-2221, the generic standard on printed board design [19]. Voltage restrictions per material limit the minimum spacing between conductors depending on an experimentally derived non-linear relationship with peak voltage. These limits can be mitigated by increasing the distance between traces, the thickness of layers between conductors, and separating phases with layers or individual PCBs.

In printed circuit boards with FR4 laminate, the relationship between current, temperature change, and cross-sectional area are also defined in IPC-2221 as:

$$I = m(\Delta T)^{0.44} (1550 \cdot A)^{0.725} \quad (3)$$

where m is a constant of either 0.048 for two-layer boards and external facing layers or 0.024 for internal layers, ΔT is the

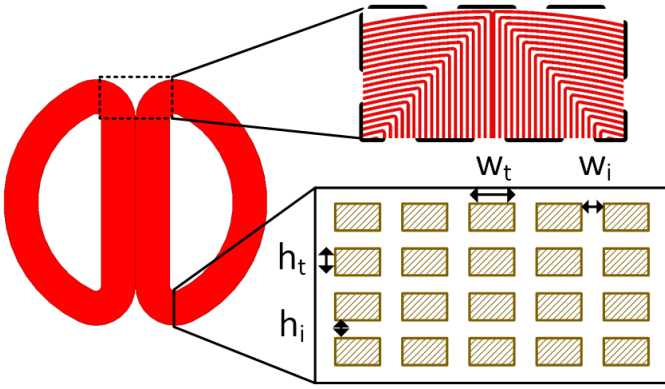


Fig. 6. Top-down view of a trace-by-trace coil with detailed views of the PCB traces and cross-section with annotated parameters.

temperature change in $^{\circ}\text{C}$, and A is the cross-sectional area in mm^2 . A summary of maximum currents varying copper thickness and layer number are presented in Fig. 5 for a trace width of 0.22mm and without forced cooling.

The maximum current increases with additional copper thickness in line with expectations due to increases to cross-sectional copper area. The largest standard thickness provided by manufacturers is 3Oz. copper as the cost and difficulty of manufacturing increases significantly beyond that. Copper thickness resulting from 6Oz. plating is the closest to the skin depth at 0.21 mm and has substantially improved thermal performance. One interesting observation is that a 3Oz. board with only two layers may have significantly better thermal performance than a 3Oz. board with multiple layers in part due to direct air contact rather than heat trapped between layers.

To apply these manufacturing constraints in an example 100mm design, the trace width is selected at 0.22mm and a trace thickness of 0.21mm with 6Oz. copper plating, both just below copper skin depth at 85kHz. The maximum current per trace in an internal layer is 2Arms with a maximum temperature change of 20°C and natural cooling. A peak voltage difference of 500V can be considered between layers in the three-phase PCB, which requires less clearance than the standard 0.254mm structural layer thickness. Assuming phases are sequentially layered and interleaved in the same PCB with no parallel connections, the maximum three-phase power with FR4 is approximately 550W with a mutual inductance of $56.8\mu\text{H}$, 72 turns per phase at 70% coil coverage.

The configuration of layer-to-layer connections can greatly improve PCB performance by allowing for more turns per phase or additional current capability with set trace dimensions. Series connections can increase the number of turns per phase for the rated mutual inductance and have naturally balanced voltages between layers. Parallel connections can be implemented within the same plane or across multiple layers to increase the effective cross-sectional area and current capability. Radial parallel splits, like that proposed in [20], are the equivalent of parallel wires or strands in hand and allow for a trade-off between resistive losses and eddy current losses

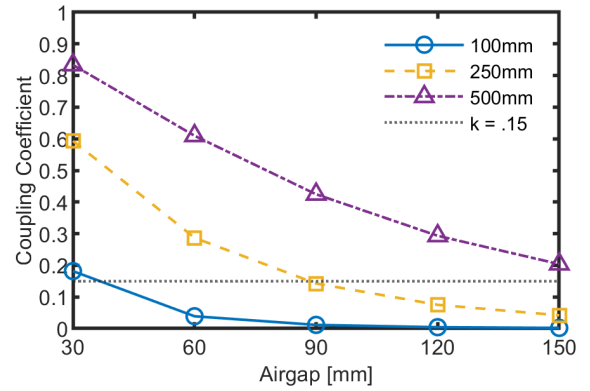


Fig. 7. Variation of the absolute value of coupling coefficient for three outer diameters. A typical value of 0.15 coupling coefficient is considered acceptable by most references.

relative to the size of the copper cross-section. The addition of parallel paths, connecting coils in parallel across multiple layers as explored in [21], [22], can increase circulating currents due to differences in induced voltages with varying proximity to the ferrite core.

One potential advantage of PCB coils is the large number of turns possible per layer due to the small conductor size and configurability, which can be estimated with the following:

$$N_{max} = \frac{(OD/2) \cdot C_c}{w_t + w_i} \quad (4)$$

where C_c is the coil coverage, the ratio of coil inside the outer diameter covered with copper conductor, w_i , the insulation width, and w_t , the trace width. An increased number of turns increases the self and mutual inductances accordingly as well as the Ampere-turns, requiring a reduced current for the same rated power. As the self-inductance increases, a smaller tuning capacitor is required with series-series compensation. For the same rated power, a trade-off then exists for higher current and associated losses or a larger number of turns, reducing the compensation capacitor size but can increase the voltage and inductance imbalance in multi-phase coils.

IV. POLYPHASE COUPLER WPT COIL CASE STUDY

Methods of simulation for the chosen geometry do not benefit from symmetry for axisymmetric modeling, like that employed in many of the previous PCB WPT papers, and may be impacted by interphase coupling, such that all three phases need to be simulated concurrently. The resulting full model has a high computational complexity due to the number of conductor paths spread across layers and turns and does not benefit from specialized developments for simplified Litz wire modeling using macro coil geometry.

The macro coil representation for PCBs, shown in Fig. 6 and proposed in Han *et al.* [23], was used to significantly reduce computational time. Macro coil height and width are determined as the product of the number of layers, trace height, h_t , and insulation height, h_i , and the product of the number of turns, trace width, w_t , insulation width, w_i , respectively.

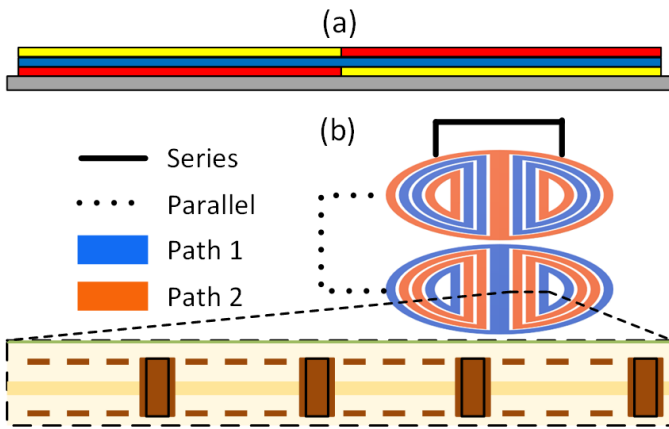


Fig. 8. Example interleaving to balance phases (a) and layer-to-layer transposition for a single phase (b). Note the alternating groups of coils connected such that the average path is the same relative to the ferrite.

Frequency domain electromagnetic 3D FEA was used with ANSYS Maxwell [24] to evaluate the coupling coefficient, inductances, and open circuit induced voltage in the secondary.

The 3-phase rotating field PCB coupler coil was designed for a 85kHz, 11kW system with 100mm OD, to serve as a small-scale example for a laboratory prototype, and a paper study for scalability up to 500mm OD. Copper trace dimensions were selected as 0.22mm width to minimize eddy current with the highest standard copper plate volume of 3Oz. or 0.108mm thickness. As the minimum gap between traces increases with thicker copper and insulation limits must be met, 0.25mm gap between planar traces and 0.1mm between layers were considered. A 70% coil coverage can be maintained for both designs by increasing the spacing between traces for the maximum coupling coefficient. The ferrite OD is 6% larger than coil OD similar to experimental prototypes with Litz wire from [8] ferrite height of 3mm was selected equal to the thickness of the PCB stack. The dimensions were the same for the primary and secondary coils to provide the best case scenario for coupling.

Imbalanced induced voltage can cause large currents between the three phases due to the relatively low resistance and imbalances in self-inductance can lead to significant increases in cost due to varying capacitor size per phase. Simulation of the straightforward sequential layer implementation, one set of PCBs for each phase stacked each other as shown in the bottom of Fig. 1, resulted in a voltage imbalance of 1Vrms in 346Vrms and a variation of $30\mu\text{H}$ in $430\mu\text{H}$ between coil self-inductances. An example approach of phase to phase balancing relative to the ferrite is shown in Fig. 8(a), wherein two of the phases are interleaved in eight layers within the same PCB on both sides of an additional eight layer PCB of the third phase.

Results for a parametric study of airgap length at multiple ODs are shown in Fig. 7 and indicate that an airgap to OD ratio of 0.3 for this geometry results in a coupling coefficient of 0.2. An airgap of 30mm was selected for the 100mm OD design with 72 series turns out of the 74 maximum number of turns per layer at 70% coil coverage. To reach rated power, a primary

phase current of 5.66Arms is necessary following simulation of the mutual inductance. Multiple parallel connections are required to keep the current density at a value suitable for the type of natural or forced cooling in the system.

At a coupling coefficient of 0.2, the 500mm OD design can have an airgap of 150mm and, at the same number of turns, would require a primary phase current of 2.12Arms for 11kW operation. Using a similar connection as in Fig. 8(b), the number of turns can be split between layers connected in series to allow for increased radial parallel splits alongside the axial parallel layer connections. For example, in the 500mm version, 4 parallel connections can be included with 2 layers, one path being the radial splits on both layers which are then connected in parallel.

V. DISCUSSION ON HIGH-POWER PCB DESIGN

Depending on the OD, layers, and phases, rated power may not be possible solely with series connections due to the limited copper thickness and widths necessary to limit eddy current losses. Circulating currents from uneven exposure of parallel paths to flux can be mitigated through transposition like that utilized for PCB stators in electric machines in Chulaee *et al.* [25]. The vias between PCB layers allows for transposition of phases in much closer proximity to the ferrite compared to wired alternatives.

An example single phase coil connection scheme is shown in Fig. 8(b), wherein two sets of turns from each coil are grouped such that the average path is the same relative to the ferrite core. These groups are then connected in parallel and transposed with respect to the outer radius for the highest likelihood of minimum imbalance between parallel paths. The combination of turn groupings and phase interleaving may be implemented to allow for parallel paths for a higher current excitation and reduced phase to phase imbalance.

Alternatively, the PCB manufacturing methods could be altered as the limiting factors for voltage and current are directly linked to the structural materials, such as FR4. Described in detail in Marcolini *et al.*, the material properties of the laminate used as insulation and structure and challenges of adding copper thickness with current manufacturing practices limit fill factor for PCBs to a maximum of 0.35 or 0.5 depending on the minimum trace width [26].

Additive copper manufacturing like that explored in Wojda *et al.* [27] have inherent benefits of reduced eddy current losses and may allow for a higher fill factor when used with insulating materials of a higher dielectric strength and thermal conductivity. Additionally, while coil size and rated power benefit from the 85kHz frequency standard, PCB coils operating at lower frequencies, such as 22kHz, can have significantly larger conductor cross-sectional area. Reducing the frequency necessitates a much larger outer diameter for the same power but could have advantages in cost and volume compared to Litz wire alternatives.

Experimental prototypes are in design for an unconventional high-power PCB coil designed with all possible techniques for wiring with axial parallel paths and radial parallel splits, phase

interleaving, and layer transposition. An experimental setup is under development for the system shown in Fig. 3 employing GaN switches and series-series compensation to evaluate coil performance relative to simulated FE studies.

VI. CONCLUSION

A 3-phase, rotating field polyphase coil with balanced fully pitched pole coverage is proposed for implementation with PCB coils which is not possible with conventional Litz wire coils. The unique capabilities of PCB manufacturing allow for a larger number of turns, parallel planar splits, transposition, and layer to layer interleaving. A specialized design procedure is developed considering limitations of PCB coils and may be used to investigate the frequency to power to dimension correlation. A polyphase coil is designed with the proposed procedure for 85kHz, 11kW operation with a scaled down lab demo at 100mm OD, 30mm airgap with studies of scalability up to 500mm OD, 150mm airgap. Coupling between the primary and secondary is evaluated using ANSYS Maxwell 3D FEA and employed in a variety of parametric studies for initial sizing. Discussion is included for methods to increase power ratings in PCB coils using a mixture of layer stacking, coil and layer connections, and material selection.

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