Transistor-Clamped Multilevel H-Bridge Inverter in Si and SiC Hybrid Configuration for High-Efficiency Photovoltaic Applications

Yibin Zhang
SPARK Lab, ECE Dept.
University of Kentucky
Lexington, KY, USA
yibin.zhang@uky.edu

Jiangbiao He
Electric Power Organization
GE Global Research
Niskayuna, NY, USA
jiangbiao.he@ge.com

Sanjeevikumar Padmanaban
Department of Energy Technology
Aalborg University
Esbjerg, Denmark
san@et.aau.dk

Dan M. Ionel
SPARK Lab, ECE Dept.
University of Kentucky
Lexington, KY, USA
dan.ionel@uky.edu

***Abstract*—Using wide bandgap (WBG) devices has been a promising solution to improve the efficiency of power inverters for photovoltaic (PV) applications. However, for multilevel inverters, using WBG devices to improve the inverter efficiency can increase the system cost dramatically due to the high price of WBG devices in the present market as well as the large number of power devices typically required in multilevel inverter topologies. In this paper, a five-level transistor clamped H-bridge (TCHB) inverter will be further investigated. This inverter requires much lower number of semiconductor switches and fewer isolated dc sources than the conventional cascaded H-bridge inverter. To improve the inverter efficiency, semiconductor switches operating at carrier frequency will be configured by Silicon Carbide (SiC) devices to reduce the dominant switching losses, while the switches operating at fundamental output frequency (i.e., grid frequency) will be constituted by Silicon (Si) devices. As a result, both of the peak efficiency and California Energy Commission (CEC) efficiency of the TCHB inverter are significantly improved and dramatic system cost increase is avoided. In addition, due to the faster saturation characteristic of the IGBT devices, the large short-circuit current in SiC MOSFETs is constrained under the condition of load short-circuit faults. In other words, this proposed "SiC+Si" hybrid TCHB inverter can ride through a load short-circuit fault. Simulation and experimental results are presented to confirm the benefits of this proposed hybrid TCHB inverter.**

***Index Terms*—Multilevel inverter, high efficiency, Silicon Carbide, hybrid configuration, photovoltaic applications.**

I. Introduction

Multilevel inverters have a number of attractive features, such as the capability of withstanding high voltage, low output harmonic distortion and dv/dt, and the like [1]. Therefore, multilevel inverters have been widely applied in various applications such as renewable energy generations, energy storage, high-voltage direct current power transmission, and medium-voltage motor drives. However, one drawback with multilevel inverters is the large number of switching devices required in their circuit topologies, which may increase the system cost and failure probability. On the other hand, to improve the efficiency of multilevel inverters especially for PV applications, using wide bandgap (WBG) devices such as Silicon Carbide (SiC) MOSFETs in multilevel inverters may not be a feasible solution in practice, due to the high cost of WBG devices and the fierce competition of solar inverters in the present market.

Recently, transistor clamped H-bridge (TCHB) multilevel inverter has received increasing interests due to the much lower number of switching devices and fewer dc sources demanded in the circuit topology [2–6], in comparison to conventional cascaded H-bridge multilevel inverters, as shown in Fig. 1 and Fig. 2, respectively. It can be seen that the TCHB inverter only consists of two major parts, namely, a neutral-point clamping circuit and an H-bridge. Typically, the neutral point clamping circuit is operated at carrier frequency, while the H-bridge is switched at much lower frequency. Particularly, the second phase leg of the H-bridge (i.e., S_4 and S_5 shown in Fig. 1) is generally modulated at fundamental output frequency (i.e., grid frequency). To improve the efficiency of the TCHB inverter, a cost-effective approach based on configuring the neutral point clamping circuit with WBG devices while keep part of the H-bridge with Silicon IGBTs will be proposed and investigated in this paper. The circuit topology of this hybrid 5-level TCHB inverter is shown in Fig. 3. As can be seen, switching devices S_1 - S_3 are configured by SiC MOSFETs, and diodes D_1 - D_4 are constituted by SiC Schottky barrier diodes (SBD). The rest switches, $S_4 - S_5$, will be configured by low-cost Si IGBTs. The advantages and performance of such a hybrid TCHB inverter will be presented in other following sections.

The remainder content of this paper is organized as follows. In Section II, the operating principle of this "SiC+Si" hybrid TCHB inverter will be introduced. In Section III, power device specifications, thermal modeling, and efficiency simulation of a five-level TCHB inverter will be presented. In Section IV, experimental implementation and verification of the five-level TCHB inverter will be detailed. Finally, conclusions will be given in Section V.

II. The Proposed "SiC+Si" Hybrid Transistor Clamped H-Bridge Inverter

The circuit topology of a five-level TCHB inverter is shown in Fig. 1. As can be seen, the neutral-point clamping circuit,

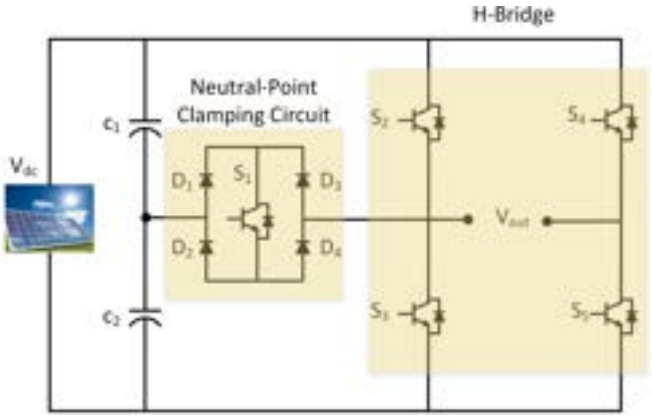


Fig. 1. Topology of a 5-level TCHB inverter.

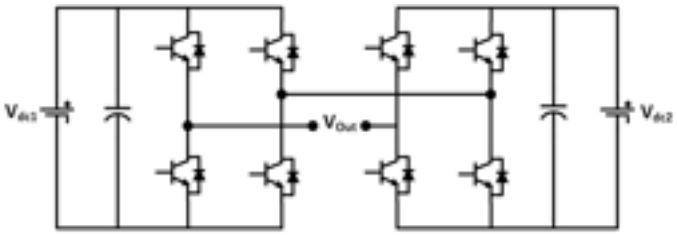


Fig. 2. Topology of a 5-level cascaded H-bridge inverter.

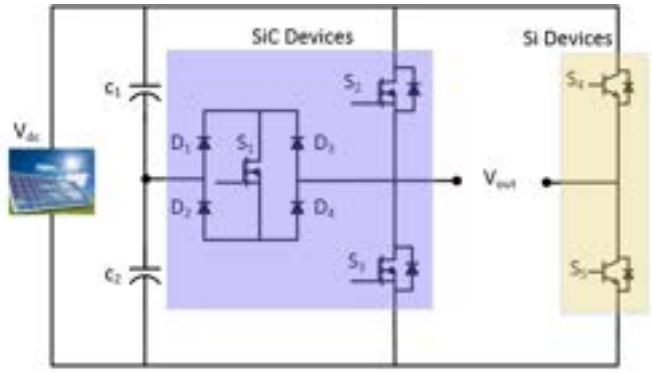


Fig. 3. The proposed "SiC+Si" hybrid 5-level TCHB inverter.

constituted by four diodes and one switch, generates voltage levels of V_{in}/2 and $(-V_{in})$/2. Accordingly, five-level voltage outputs can be obtained from the TCHB inverter, namely, V_{in}, V_{in}/2, 0, $(-V_{in})$/2, and $-V_{in}$, by providing proper switching patterns to the switches. S_4 and S_5 are operated at fundamental frequency, while the switches S_1 - S_3 will be switching at much higher carrier frequency.

In this paper, considering that SiC devices have much lower switching losses than their Si counterparts due to their wide bandgap material characteristics [7, 8], SiC MOSFETs are employed for the high-frequency switches S_1 - S_3 to improve the efficiency of the TCHB inverter, while the low-frequency switches S_4 and S_5 are still configured by the low-cost Si IGBTs, as illustrated in Fig. 3. The following sections will confirm the advantages and performance of this proposed hybrid TCHB inverter with simulation and experimental results.

III. Modeling and Simulation of the Proposed Hybrid TCHB Inverter

To evaluate the efficiency improvement and other performance of the "SiC+Si" hybrid TCHB inverter, thermal modeling of a single-phase 5-level TCHB inverter has been conducted in ANSYS Simplorer software environment, and the associated simulation results are presented and discussed as follows.

A. Sizing of the 5-level TCHB Inverter

The simulation modeling is based on a single-phase 5-level TCHB inverter used for PV applications, with a rated power of 500W. The nominal dc bus voltage is 120V deriving from four series connected PV panels, with each rated at 30V. An RL load is interconnected between the two phase legs (R_{load} =100Ω, L_{load} =12mH). The rated fundamental frequency is 50Hz, and the carrier frequency is set at 1kHz. Infineon IGBTs IKP08N65H5 [9] (650V/12A, integrated with soft antiparallel diodes) are selected for S_4 - S_5 and their freewheeling diodes in the proposed TCHB inverter. Also, SiC MOSFETs (Rohm SCT3120AL, 650V/15A) are selected for all the switches operated close to the carrier frequency, and SiC Schottky barrier diodes (Rohm SCS212AJHR, 650V/12A) are used for all the four clamping diodes in the TCHB inverter [10]. Based on the device thermal modeling, the comparison of the efficiency and other performance between the all-Si TCHB inverter and the proposed hybrid TCHB inverter will be simulated and presented as follows.

B. PWM Modulation

Regarding the PWM strategies, the existing PWM method for the TCHB inverter has been developed and is named as Single Reference Double Carriers (SRDC) method [2], as shown in Fig. 4a. However, as reported in [11] such SRDC method has a higher Total Harmonic Distortion (THD) under certain conditions. Therefore, in this paper, a Double Reference Single Carrier (DRSC) PWM method is adopted, which has better THD performance [11].

The modulation index is defined as follows:

$$m = \frac{V_{ref}}{2V_{Cr}} \tag{1}$$

where V_{ref} and V_{Cr} represent the amplitude of the voltage reference and the amplitude of the carrier signal, respectively.

The switching period Δt can be calculated by:

$$\Delta t = \frac{2\pi f_1}{f_s} \tag{2}$$

where f_1 and f_s represent the fundamental frequency and the switching frequency, respectively. In every switching period, the average voltage can be calculated by:

$$\overline{V} = 2V_s \frac{2\delta - \Delta t}{\delta} \tag{3}$$

where the upper voltage V_s is over the period of δ and the $-V_s$ is for the period $(\Delta t - \delta)$, respectively.

If the reference voltage can be defined as:

$$v_{ref} = V_m sin\theta \tag{4}$$

then, the volt-second area A can be obtained by integrating (4), when the period δ is small enough. On this basis, the switching angle can be obtained as:

$$\delta_{sw} = (\Delta t/4) + (\Delta t/4) M sin(t - \delta) \tag{5}$$

However, such a PWM modulation method has certain drawbacks especially at light load conditions, such as the degradation of the efficiency and the THD. As a result, the DRSC PWM method is employed here, as shown in Fig. 4b.

Similar to the development of the SRDC PWM method, reference v_{ref1} and v_{ref2} can be derived from a full sinusoidal voltage reference. As a result, the voltage reference is defined as:

$$v_{ref} = V_{ref} sin\theta \tag{6}$$

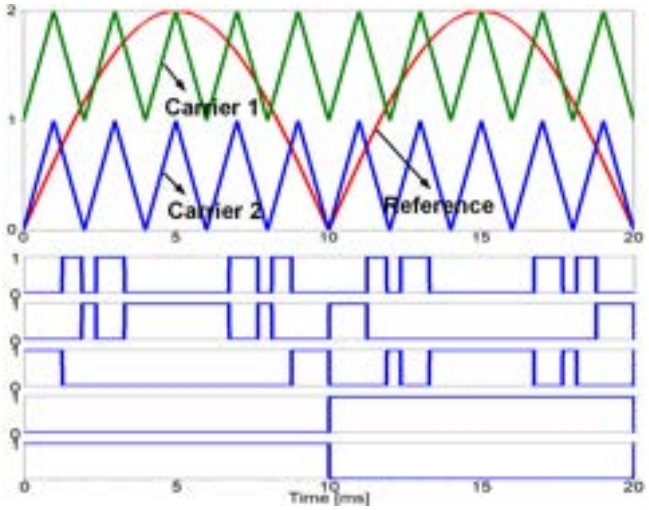
$$v_{ref1} = |1 - v_{ref}| \tag{7}$$

$$v_{ref1} = |2 - v_{ref}| \tag{8}$$

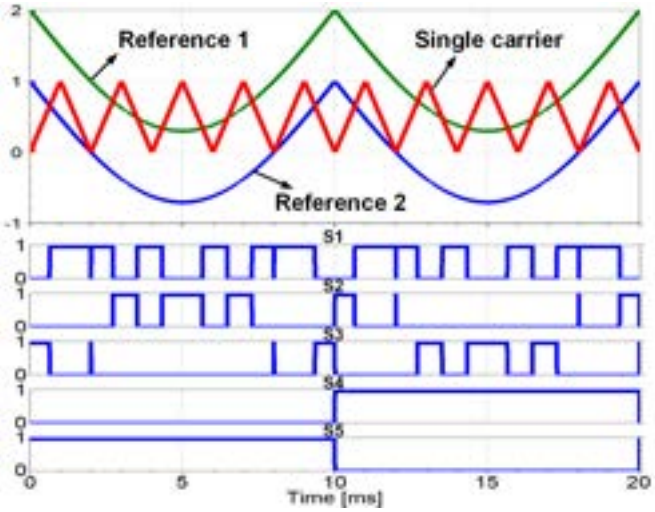
Specifically, two rectified sinewave reference signals and one triangular carrier signal are utilized in this modulation scheme. When the triangular carrier signal is between the two rectified sinewave reference signals, the switch S_1 is turned on and turned off otherwise. The switch S_2 is turned on when the carrier signal is higher than the reference-1 signal in first half period or lower than the reference-2 signal in the second half period. The switch S_3 is turned on when the carrier signal is lower than the reference-2 signal in first half period or higher than the reference-1 in the second half period. As shown in Fig. 4b, S_4 and S_5 are operated at a fundamental frequency, while the switches S_1 - S_3 will be switching at a much higher carrier frequency.

C. PV Array and MPPT Modeling

A solar array with the maximum power point tracking (MPPT) strategy is modeled based on SunTech Power STP235-20 which provides 170V/850W at the maximum power point [12]. Fig. 5a shows the typical current-voltage (I-V) and power-voltage (P-V) curves of the modeled PV array at $1000W/m^2$ of irradiation and 25 °C temperature. The MPPT controller tracks the output voltage and power by following the P-V and I-V curves when there is partial shading and the solar irradiance drops. The controller performance is studied as shown in Fig. 5b, where irradiance drops from 1000 W/m^2 to 400 W/m^2 at 0.4 seconds of the simulation time. With the MPPT controller, the reference dc voltage tracks the PV output voltage which is then provided to the single stage inverter.



(a)

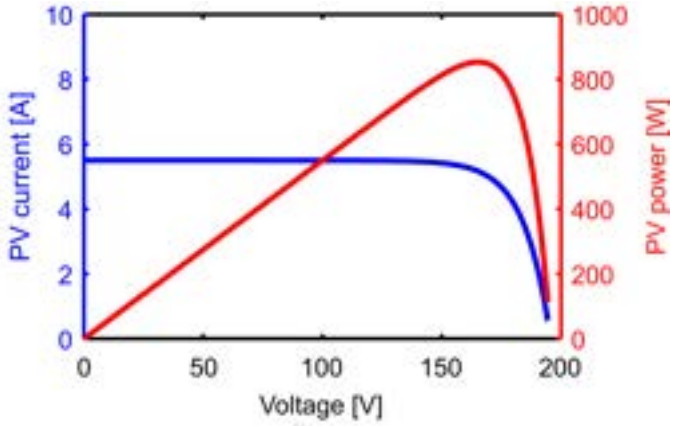


(b)

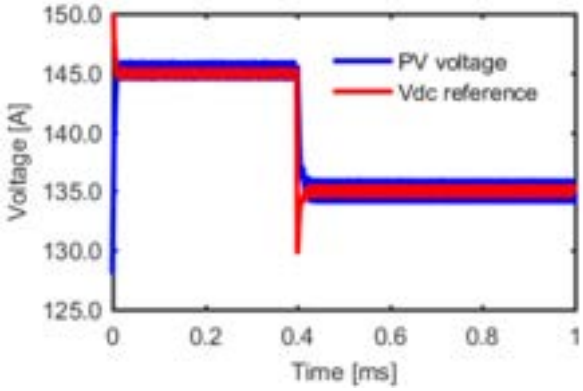
Fig. 4. The PWM modulation strategies. (a) Single reference double carrier (SRDC). (b) Double reference single carrier (DRSC)

D. Efficiency Simulation

First of all, the normal output of the proposed hybrid 5-level single-phase TCHB inverter is simulated at unity modulation index, and the results are shown in Fig. 6. Fig. 6 depicts the five-level line voltage, output current of the TCHB inverter at RL load. The comparison of the conduction losses and switching losses in each semiconductor device at rated power between the all-Si TCHB inverter and the proposed hybrid TCHB inverter are simulated and shown in Fig. 7a-7b, respectively. It should be noted that the neutral point clamping circuit that is composed of four SiC diodes and one SiC MOSFET (as shown in Fig. 3) is updated with two anti-series-connected SiC MOSFETs in the simulations of the hybrid TCHB inverter, which can further reduce the device losses and improve the inverter efficiency. It can be seen that both the conduction and switching losses are reduced in the proposed hybrid TCHB inverter. Particularly, the switching loss in the



(a)



(b)

Fig. 5. The PV characteristics and the MPPT implementation (a) The I-V and P-V characteristics. (b) The PV voltage and DC reference voltage with various irradiance.

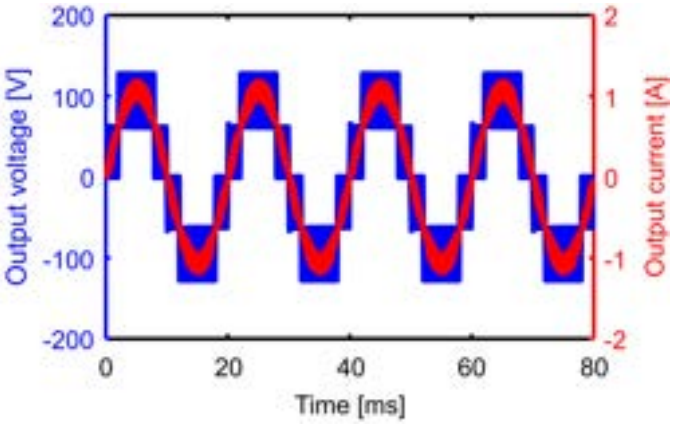
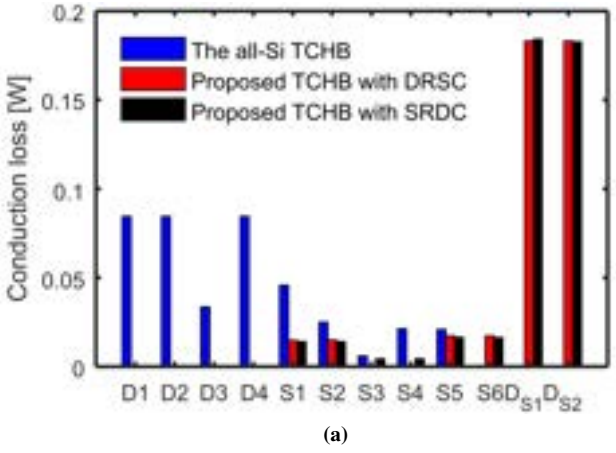
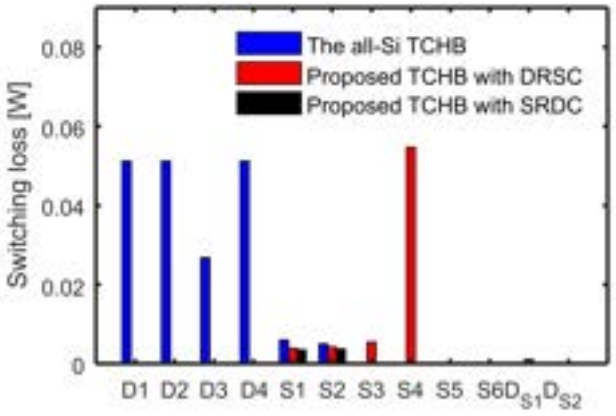


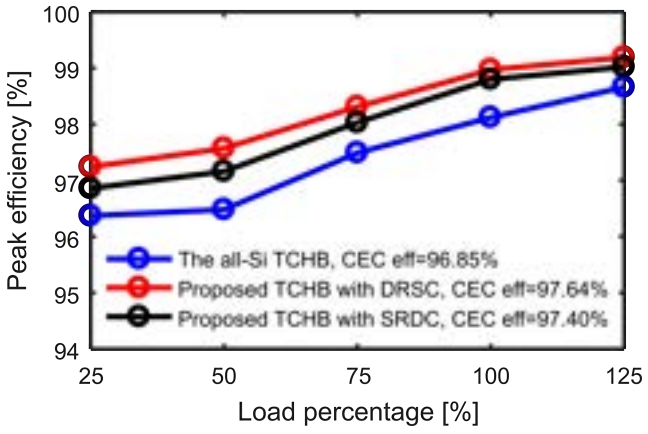
Fig. 6. The output voltage and current with RL load.



(a)



(b)



(c)

Fig. 7. Comparison of the power device losses and inverter efficiency between the all-Si TCHB inverter and the proposed hybrid counterpart (a) conduction losses (b) switching losses (c) inverter efficiency at various load levels.

S_1 of the convetional all-Si TCHB inverter is much larger than the one in the proposed hybrid TCHB inverter, mainly due to the high carrier frequency operation of S_1 in the all-Si inverter which generates significant switching losses. As a result, the efficiency comparison based on the simulated device losses are shown in Fig. 7c, which illustrates that the proposed hybrid TCHB inverter with DRSC can achieve higher peak efficiency and higher California Energy Commission (CEC) efficiency. Specifically, at the nominal load condition, the proposed TCHB inverter based on the DRSC modulation method achieves a peak efficiency of 98.97% which is 0.85% higher than the all-Si TCHB inverter and 0.17% higher than

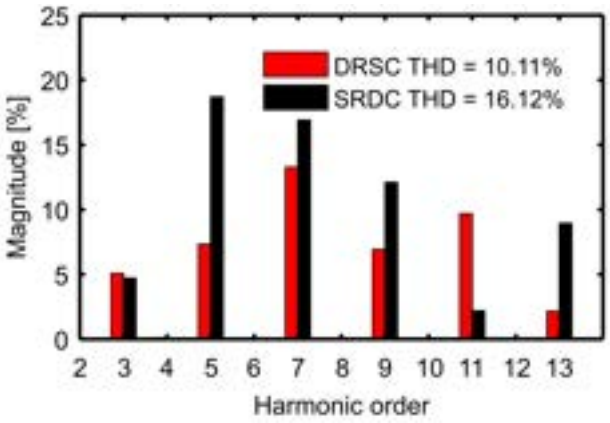


Fig. 8. The voltage harmonics and THD at unity modulation index.

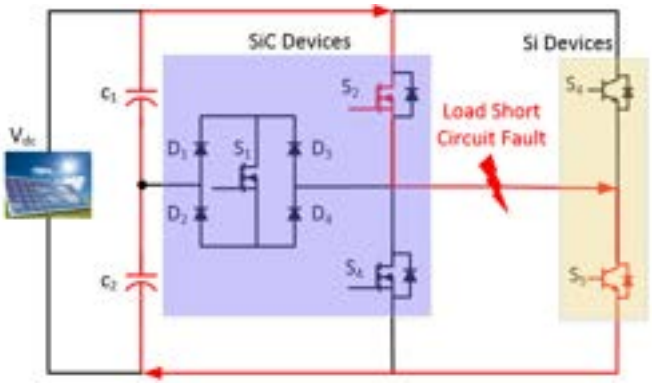


Fig. 9. Current flow direction during a load short-circuit fault.

the hybrid TCHB inverter based on the SRDC at the same operating conditions. As for the CEC efficiency, the proposed TCHB inverter modulated by the DRSC method can achieve 97.64% CEC efficiency, which is 0.79% higher than the all-Si TCHB and 0.24% higher than the hybrid TCHB inverter based on the SRDC method. Besides, the output voltage harmonics and the THD are investigated for the proposed TCHB inverter modulated by the DRSC and the SRDC PWM methods, respectively, and the simulated results are shown in Fig. 8. With the conventional SRDC modulation method, the THD value for the TCHB inverter is 16.12%, while the THD value based on the DRSC PWM strategy is reduced to 10.11% under the same operating condition.

E. Simulation of Load Short-Circuit Behavior

Compared with IGBTs which can typically withstand 10μs of short-circuit current, SiC MOSFETs have much weaker short-circuit capability, mainly due to the higher saturation current level and smaller physical size of the device die chips. Such issue becomes even worse when the commutation loop inductance of the power inverter is minimized to reduce switching losses, since it facilitates a much higher increase rate of the short-circuit current, leaving very short time for the over current protection circuit to react. However, super-fast short circuit protection requirement, such as 0.5-1μs, is very challenging and may introduce additional problems, such as EMI noise susceptibility and the like.

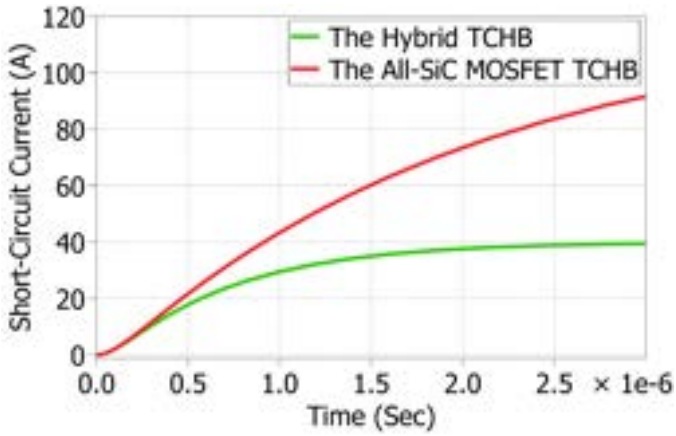


Fig. 10. Comparison of the short-circuit current between the "SiC+Si" hybrid TCHB inverter and the all-SiC TCHB inverter.

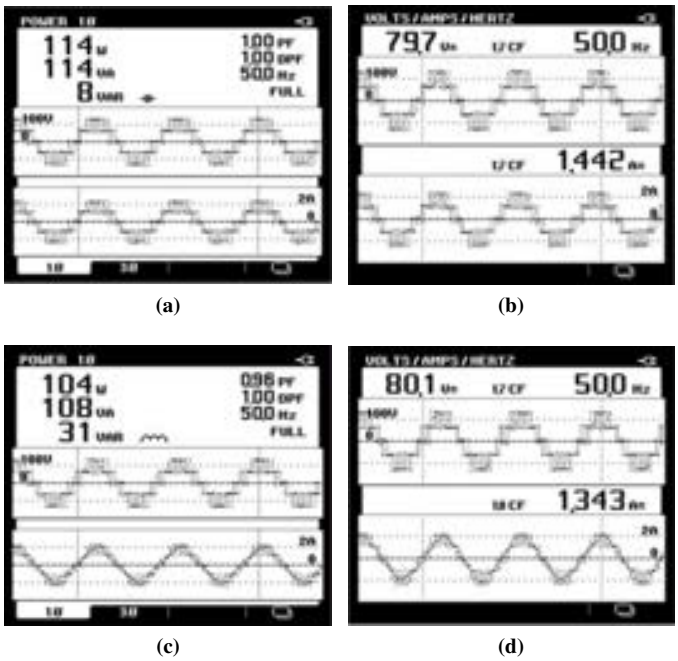
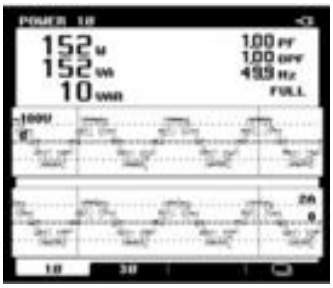
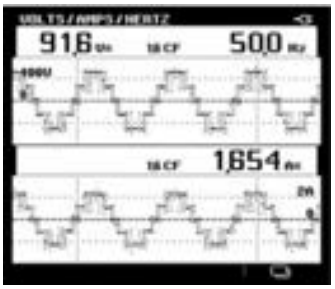


Fig. 11. The measured output performance of the TCHB inverter at m=0.85 (a) Output power with R-load. (b) Output voltage and current of the TCHB inverter with R-load. (c) Output power of the TCHB inverter with RL-load. (d) Output voltage and current of the TCHB inverter with RL-load.

In this proposed 5-level TCHB inverter, the SiC MOSFETs can withstand more than 10μs of short-circuit current, without any additional short-circuit current protection scheme in the gate drivers. Such unique benefit results from the hybrid configuration of the SiC MOSFETs and Si IGBTs in the proposed inverter. As illustrated in Fig. 9, when the fault current flowing through SiC MOSFETs during a load short-circuit fault, the short-circuit current flowing through the SiC MOSFET S_2 will be constrained by the faster current saturation in the IGBT S_5.

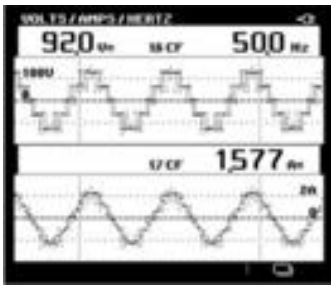


(a)



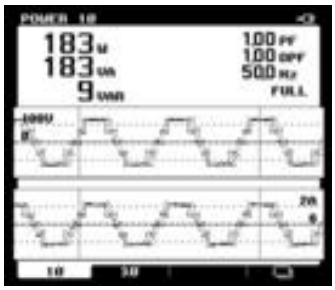
(b)

(c)

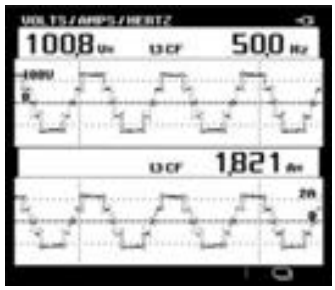


(d)

Fig. 12. Measured output performance of the TCHB inverter at m=1 (a) Output power with R-load. (b) Output voltage and current of TCHB inverter with R-load. (c) Output power of the TCHB inverter with RL-load. (d) Output voltage and current of the TCHB inverter with RL-load.

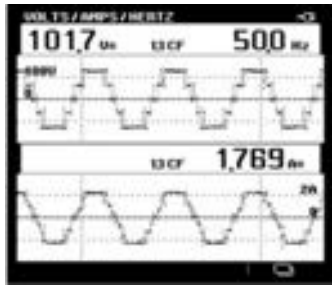


(a)



(b)

(c)



(d)

Fig. 13. Measured output performance of the TCHB inverter at m=1.25 (a) Output power with R-load. (b) Output voltage and current of TCHB inverter with R-load. (c) Output power of the TCHB inverter with RL-load. (d) Output voltage and current of the TCHB inverter with RL-load.

The comparison between an all-SiC-MOSFET TCHB inverter and the proposed "SiC+Si" TCHB inverter under the same load short-circuit fault is simulated and shown in Fig. 10. As can be seen, the short-circuit current is constrained at 40A in the proposed hybrid inverter, much lower than the short-circuit current of the all-SiC-MOSFET counterpart. In other words, the proposed hybrid TCHB inverter can ride through such a load short-circuit fault due to the faster saturation characteristics of the Si IGBTs in the inverter.

IV. Experimental Verification

A single-phase five-level TCHB inverter was designed and implemented in the laboratory. The input dc supply is provided by four series connected PV panels, with each rated at 32V. Each PV panel has an open-circuit voltage of 39.5V and a short-circuit current of 2A. The switching frequency of the TCHB inverter is set at 1 kHz, while the fundamental output frequency is set at 50 Hz. On the load side, a power resistor rated at 100/500W resistor and 12 mH inductor are utilized to configure the load either as a pure resistive load or as an RL load.

The output performance of the proposed hybrid TCHB inverter is the same as all-Si counterpart, and the main difference between them is the loss dissipation and efficiency. Here, the output performance of an all-Si 5-level TCHB inverter is provided to confirm the operating principle of the inverter. Fig. 11a-11d show the measured output power, output voltage and current at R-load and RL-load, at the modulation index of m=0.85. As can be seen that the output power of the TCHB inverter at pure resistive load is 114W, and their output voltage and current are 79.7V and 1.44A, respectively. At an RL load, the input power is 104W, and the associated output voltage and current are 80.1V and 1.343A, respectively. Likewise, Fig. 12a-12d show the measured output power, output voltage and current at R-load and RL-load at unity modulation index (i.e, m=1). Similarly, Fig. 13a-13d show the measured output power, output voltage and current at R-load and RL-load at over modulation index (i.e, m=1.25). All these experimental results confirm the operation and function of the five-level single-phase TCHB inverter.

V. Conclusion

In this paper, a cost-effective approach based on a hybrid utilization of SiC and Si devices was proposed to improve the efficiency of a multilevel TCHB inverter. Specifically, the auxiliary neutral-point voltage clamping circuit which is operated at high carrier frequency is configured with SiC devices, while the H-bridge inverter switched at low fundamental frequency is constituted with Si devices. Simulation and thermal models of the all-Si single-phase five-level TCHB inverter and the proposed "SiC+Si" hybrid counterpart are developed in ANSYS Simplorer. Simulation results show that the peak efficiency of the inverter can be improved by 0.85% at the nominal operating condition, compared to all-Si TCHB inverter under the same operating conditions. Also, the CEC efficiency of the proposed hybrid TCHB inverter can be

improved by 0.79% compared to all-Si TCHB inverter at the same conditions. Furthermore, the THD performance based on both the PWM methods of SRDC and DRSC strategies were investigated for the TCHB inverter, and the comparison shows that the DRSC modulation strategy yields lower THD value. Another advantage is that, compared to all-SiC-MOSFET based TCHB inverter, the proposed hybrid TCHB inverter can ride through a load short-circuit fault due to the faster saturation characteristics of Si IGBTs constraining the short-circuit current in the inverter. Experimental results are presented to confirm the performance of the TCHB inverter at various operating conditions.

ACKNOWLEDGMENT

The support of University of Kentucky, the L. Stanley Pigman endowment and the SPARK program, and ANSYS Inc. is gratefully acknowledged.

REFERENCES

[1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug 2002.

[2] N. A. Rahim, M. F. M. Elias, and W. P. Hew, "Transistor-clamped h-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 8, pp. 2943–2956, Aug 2013.

[3] M. F. M. Elias, N. A. Rahim, H. W. Ping, and M. N. Uddin, "Asymmetrical cascaded multilevel inverter based on transistor-clamped h-bridge power cell," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 4281–4288, Nov 2014.

[4] J. Lakwal and M. Dubey, "Design and implementation of an extended modular structure of transistor clamped h-bridge multilevel inverter for single dc source," *2015 International Conference on Industrial Instrumentation and Control (ICIC)*, pp. 1294–1299, May 2015.

[5] N. B. Deshmukh, R. D. Thombare, M. M. Waware, and D. S. More, "A novel family of three phase transistor clamped h-bridge multilevel inverter with improved energy efficiency," *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pp. 1–5, Dec 2016.

[6] S. P. Gautam, S. Gupta, and L. Kumar, "Reliability improvement of transistor clamped h-bridge-based cascaded multilevel inverter," *IET Power Electronics*, vol. 10, no. 7, pp. 770–781, 2017.

[7] X. She, A. Q. Huang, . Luca, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8193–8205, Oct 2017.

[8] J. He, T. Zhao, X. Jing, and N. A. O. Demerdash, "Application of wide bandgap devices in renewable energy systems - benefits and challenges," *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, pp. 749–754, Oct 2014.

[9] Infineon Inc., "Ikp08n65h5," 2017, www.infineon.com/, Accessed on 2017-12-29.

[10] Rohm Inc., "Rohm sct3120al," 2017, www.rohm.com, Accessed on 2017-12-29.

[11] M. S. Bhaskar, S. Padmanaban, V. Fedk, F. Blaabjerg, and P. Wheeler, "Transistor clamped five-level inverter using non-inverting double reference single carrier pwm technique for photovoltaic applications," *2017 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM) 2017 Intl Aegean Conference on Electrical Machines and Power Electronics (ACEMP)*, pp. 777–782, May 2017.

[12] SunTech Co., Ltd., "Suntech power stp235-20," 2017, http://www.suntech-power.com/menu/xzj-dj48p.html, Accessed on 2018-05-12.